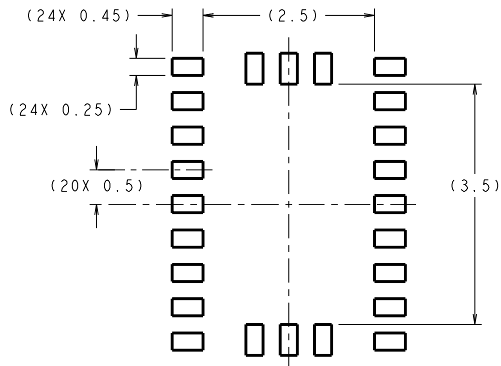
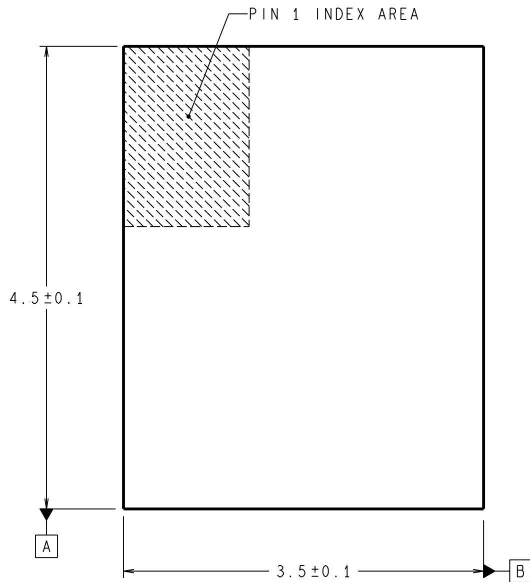
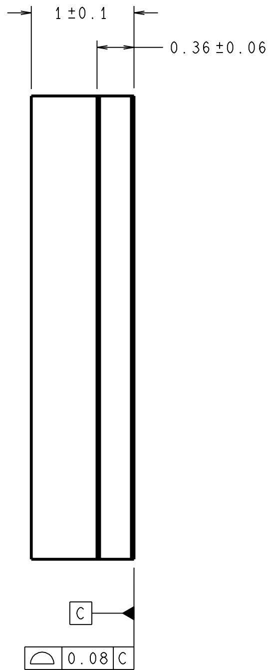
REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	11957	03/19/1998	TL/AP
B	REVISE METAL & SOLDERMASK LAYERS; PKG THICKNESS WAS 0.9-1.1; REVISE TITLE; ADD COPLANARITY TO BACK VIEW; PAD WIDTH TOLERANCE WAS 0.03	12031	06/18/1998	TL/AP
C	REVISE NOTES 2 & 3; TRUE POS TOL WAS 0.05; COPLANAR TOL WAS 0.05	12096	10/06/1998	TL/

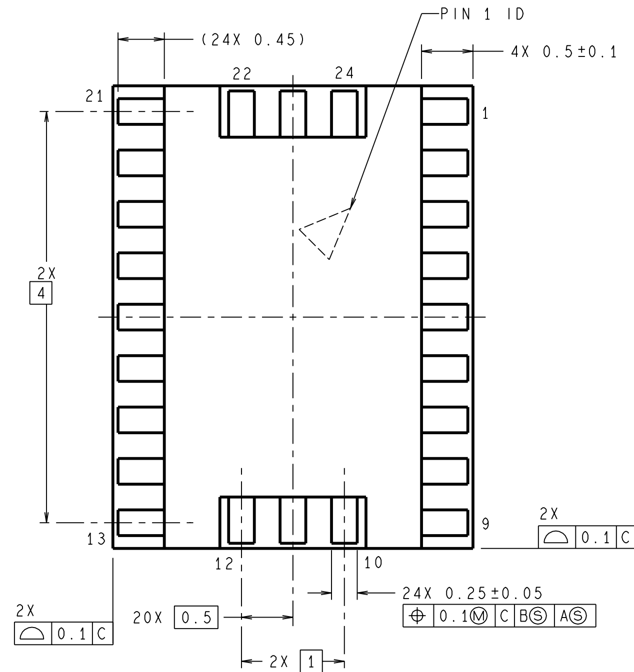


RECOMMENDED LAND PATTERN
1:1 RATIO WITH PACKAGE SOLDER PADS

DIMENSIONS ARE IN MILLIMETERS







NOTES: UNLESS OTHERWISE SPECIFIED.

1. MATERIAL: BT RESIN CCL-HL832 WITH TAIYO PSR4000 AUS5 SOLDER MASK.
2. PLATING: Cu 15 TO 20 MICROMETERS
   Ni 10 ± 5 MICROMETERS
   Au 1 ± 0.5 MICROMETER
3. REFERENCE JEDEC REGISTRATION MO-208, VARIATION ECE-1, DATED SEPTEMBER 1998.

APPROVALS	DATE	
DRAWN T. LEQUANG	03/19/1998	National Semiconductor 2900 Semiconductor dr., Santa Clara, CA 95052-8090
DFTG. CHK.		**CSP, PLASTIC, LAMINATED, 3.5 X 4.5 X 1.0 mm BODY, 24 L, 0.5mm PITCH**
ENGR. CHK.		

PROJECTION	SCALE	SIZE	DRAWING NUMBER	REV
INCH [MM]	N/A	C	(SC)MKT-SLB24A	C
	DO NOT SCALE DRAWING		SHEET 1 of 1	