4.5.8 – 144 PIN SDR SGRAM/SDRAM SO–DIMM FAMILY

NOTE: It is recommended that this module be used primarily for Graphics Memory applications. 144 P DRAM & SDRAM standards foe Main Mamory use have been adopted and are published elsewhere in JESD 21–C.

CAPACITY—up to the addressing capacity of 12 bits, address multiplexed with words of 32, & 64 bits.

DATA CONFIGURATIONS—Two DATA Word configurations are defined:
—32 BIT SGRAM or SDRAM without PARITY
—64 BIT SGRAM or SDRAM without PARITY

CONFIGURATION—4 Different Configurations are defined using X32 SGRAM or SDRAM memories in 1 and 2 bank configurations.

LOGIC FEATURES—The modules contain the Serial Presence Detect (SPD) feature (optional) that consist of a built in serial access EEPROM that stores information on mutiple parameters and attributes of the module such as technology, storage capacity, configuration, data word configuration, refresh mode, and speed of the module.

HARDWARE FEATURES—Physical layout parameters and terminating resistors are given to optimize the speed characteristics of the module. The key has been located at pin 50 and is different from the other 144 P SO–DIMM packages.

LOGIC INTERFACE LEVEL—LVTTL

POWER SUPPLY—3.3 v ± 10%

PACKAGE—144 PIN JEDEC SO–DIMM MEMORY MODULE with the Key at pin 50.

PIN ASSIGNMENTS —Figs. 4.5.8–A & 4.5.8–B

Configuration, Electrical Characteristics,SPD, & Output Measurement Ckt — P 4.5.8–4 & Fig. 4.5.8–C

Resistor Strapping Options & PCB Layout Considerations — P 4.5.8–5

QFP Clock Routing —Fig. 4.5.8–D

QFP Address and Control Routing — Fig. 4.5.8–E

QFP Data Routing — Fig. 4.5.8–F

TSOP Layout Considerations — P 4.5.8–9

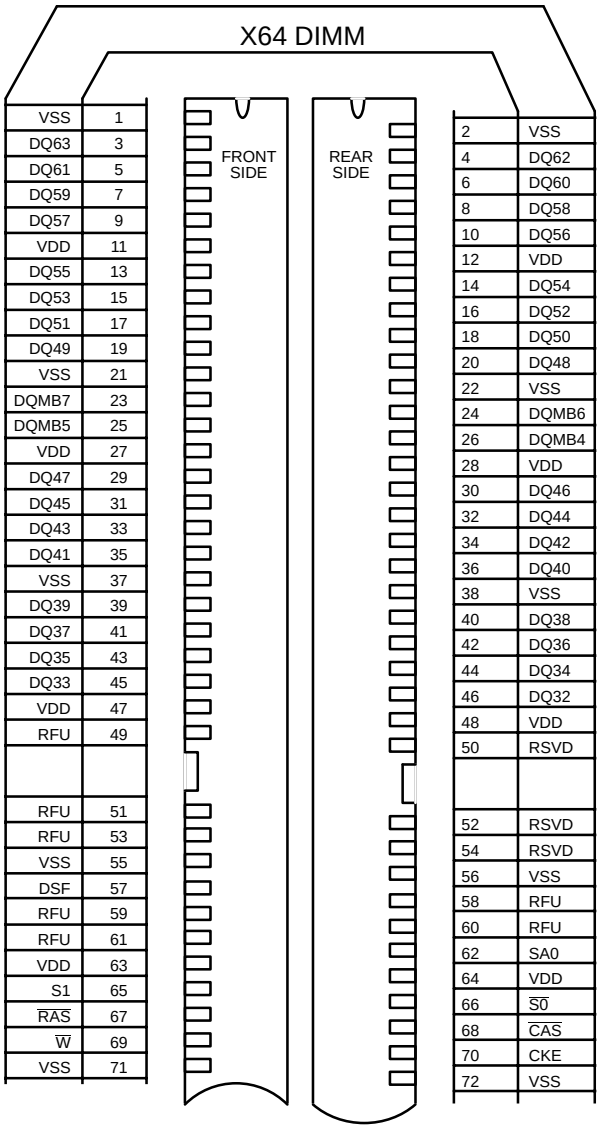
256K, 512K, 1M X 32 Block Diagram (1 bank of 1 X 32 device) — Fig. 4.5.8–G

512K, 1M, 2M X 32 Block Diagram (2 bank of 1 X 32 devices) — Fig. 4.5.8–H

256K, 512K, 1M X 64 Block Diagram (1 bank of 2 X 32 devices) — Fig. 4.5.8–I

512K, 1M, 2M X 64 Block Diagram (2 bank of 2 X 32 devices) — Fig. 4.5.8–J

The Pinout below is based on routing for QFP

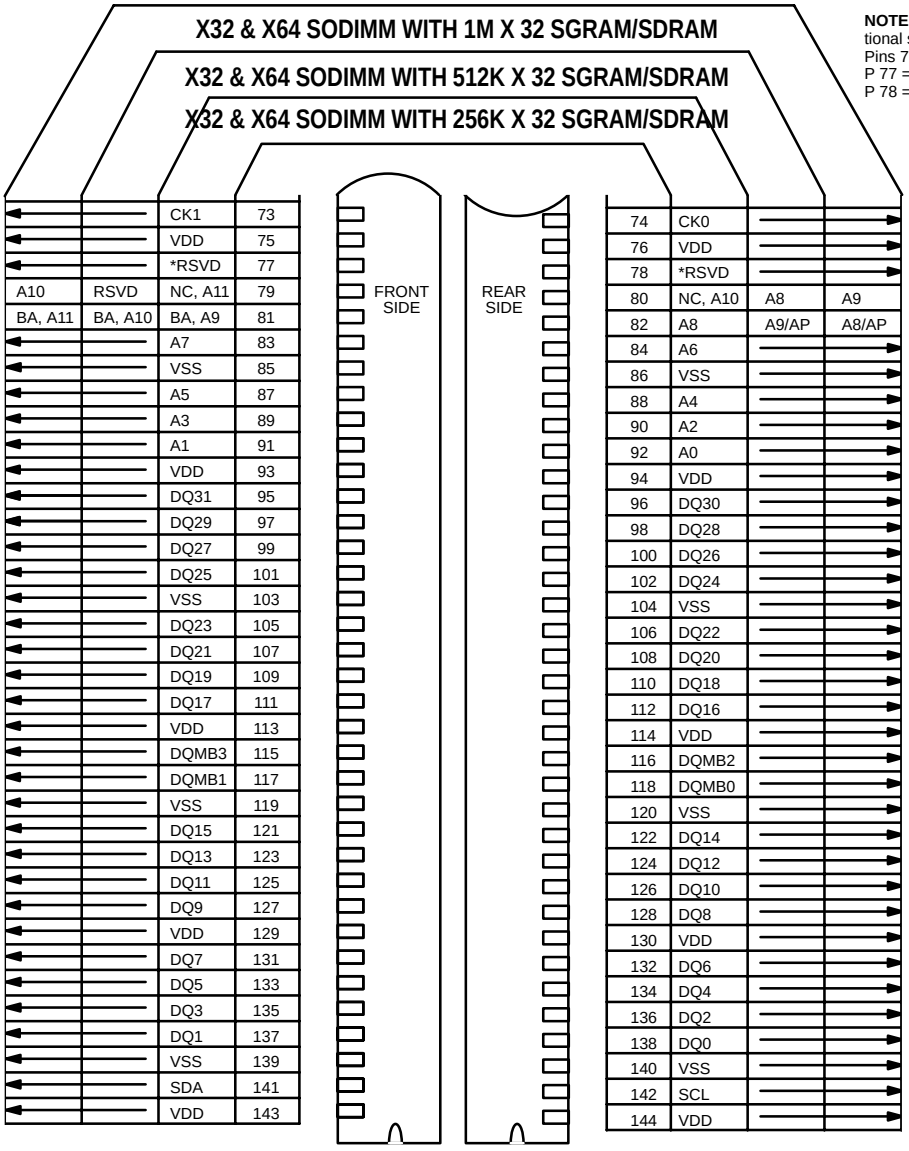


NOTE: The pins on this half of the module are the same for all capacities of SDRAM

FIGURE 4.5.8–A
144 Pin X32 & X64 SGRAM SO–DIMM, PIN ASSIGNMENTS
UPPER HALF

0

The Pinout below is based on routing for QFP



NOTE: The following optional signals are defined for Pins 77 & 78 as follows
P 77 = RSVD, $\overline{\text{MWAIT}}$
P 78 = RSVD, $\overline{\text{MIRQ}}$

FIGURE 4.5.8–B
144 PIN X32 & X64 SGRAM SO–DIMM, PIN ASSIGNMENTS
LOWER HALF

Configuration

Graphic controllers can determine the module capabilities one of three ways; they are:

- Using the default parameters with power–up testing
- Using resistor strapping options on the data lines
- Using an optional Serial Presence Detect EEPROM

Modules are required to include resistor support (3 resistors); the Serial Presence Detect EEPROM is optional.

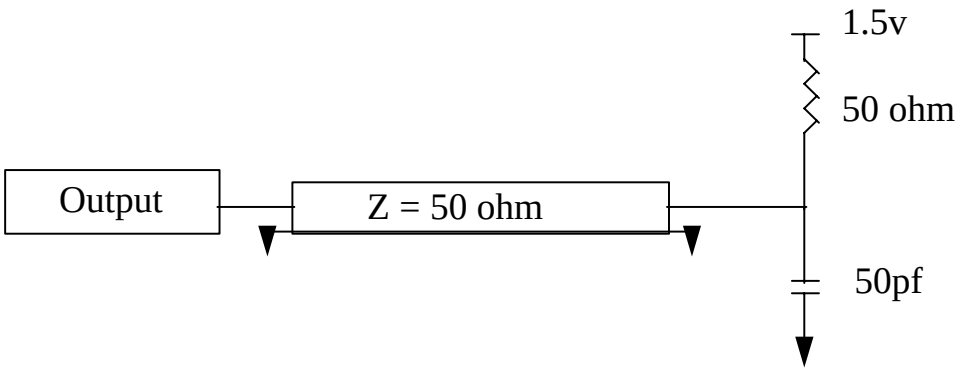
Electrical Characteristics

The module electrical characteristics are carefully controlled to allow system configurations with two separate memory arrays. This may include either two modules or one module plus memory soldered directly to the motherboard or add–in card PCB. Routing on the main board will generally be done as a T–topology. The module's electrical characteristics (as well as the main board's characteristics) must be carefully implemented to insure a balanced T–topology.

The board must have a characteristic impedance between 55 and 85 ohms.

Serial Presence Detect EEPROM

This EEPROM is optional on the module



Reference level for measurement is set at 1.4V.

FIGURE 4.5.8–C
OUTPUT MEASUREMENT LOAD CIRCUIT

Resistor Strapping Options

Three resistor straps are used to indicate the synchronous clock frequency (period) and memory timing. Timing information for each clock frequency is indicated in the section titled *Memory Timing*. Memory modules must meet all timing requirements within the specified operating environment.
☞ Paragraph border is not supported. ☜

Cycle Time	DQ31	DQ30	DQ29
15 nS	0	0	0
12 nS	0	0	1
10 nS	0	1	0
8 nS	0	1	1
reserved	1	0	0
reserved	1	0	1
reserved	1	1	0
reserved	1	1	1

A logic low (i.e. 0) indicates that the resistor strapping is tied to ground (Vss). A logic high (i.e. 1) indicates that the resistor strapping is ties to VDD. Resistors should be a 4.7K value on the DQ lines.

PCB Layout Considerations

To insure proper signal integrity, the module routing must be taken under careful considerations. This section outlines PCB layout considerations for the SO–DIMM module. It is broken into two sections; the first covers PCB layout considerations for modules based on 100–pin PQFP or TQFP SGRAM, while section two covers modules based on TSOP packages.

Each section looks at three separate topologies; one for clocks, one for control/address, and one for data.

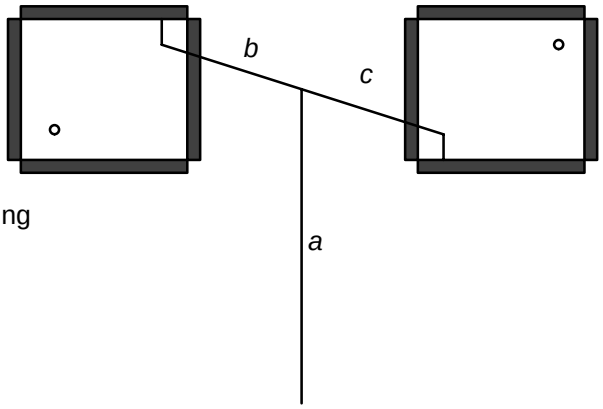
PQFP or TQFP Layout Considerations

The assumed loading for this configuration is:

Signal	32–bit		64–bit	
	Single–sided	Double–sided	Single–sided	Double–sided
clocks	1 load	1 load	2 loads	2 loads
address/control	1 load	2 loads	2 loads	4 loads
data	1 load	2 loads	1 load	2 loads

QFP Clock Routing

Clock loading is two loads per line, maximum. Routing should be performed using a T–topology, as shown in Refernce Drawing below:



Reference Drawing

The following table lists the allowable stub lengths for the clock routing.

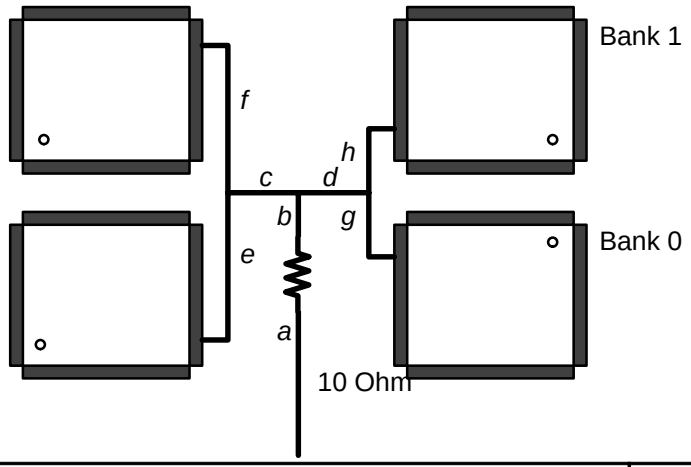
Parameters	**SDRAM/SGRAM Clock Frequency**								**Units**
	15 nS		12 nS		10 nS		8 nS		
	Min.	Max	Min.	Max	Min.	Max	Min.	Max	
a	75	150	75	150	75	150	75	150	pS
b	0	115	0	115	0	115	0	115	pS
c	0	115	0	115	0	115	0	115	pS
b+c	0	225	0	225	0	225	0	225	pS
Total Length (clock)	100	365	175	325	175	325	175	325	pS
Total Length (chip select)	0	365	0	365	0	365	0	365	pS

FIGURE 4.5.8–D
QFP CLOCK ROUTING

QFP Address/Control Routing

Address and control (CKE, /RAS, /CAS, /WE, and DSF) loading is four loads, maximum. Routing should be performed using a modified daisy–chain with T–stubs, as shown in reference drawing below:

Reference Drawing



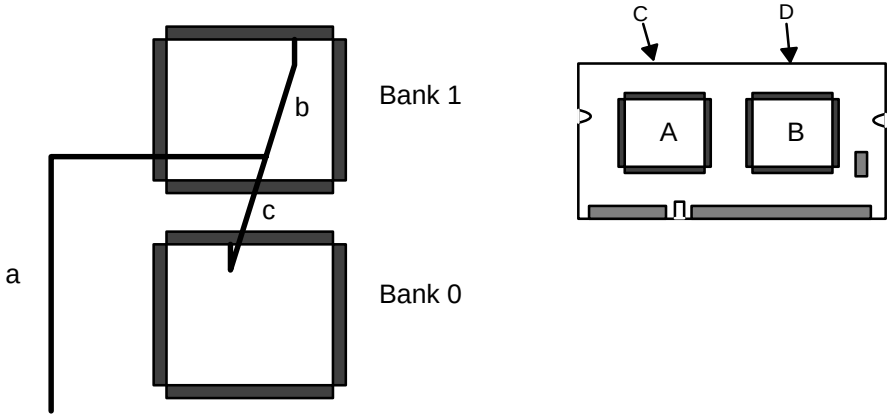
Parameters	SDRAM/SGRAM Clock Frequency								Units
	15 nS		12 nS		10 nS		8 nS		
	Min.	Max	Min.	Max	Min.	Max	Min.	Max	
a	0	37	0	37	0	37	0	37	pS
b	0	190	0	190	0	190	0	190	pS
c	0	115	0	115	0	115	0	115	pS
d	0	115	0	115	0	115	0	115	pS
e	0	115	0	115	0	115	0	115	pS
f	0	115	0	115	0	115	0	115	pS
g	0	115	0	115	0	115	0	115	pS
h	0	115	0	115	0	115	0	115	pS
b–c	–75	75	–75	75	–75	75	–75	75	pS
b–d	–75	75	–75	75	–75	75	–75	75	pS
c+e	0	190	0	190	0	190	0	190	pS
c+f	0	190	0	190	0	190	0	190	pS
d+g	0	190	0	190	0	190	0	190	pS
d+h	0	190	0	190	0	190	0	190	pS
total length	0	375	0	375	0	375	0	375	pS

FIGURE 4.5.8–E
QFP ADDRESS/CONTROL ROUTING

QFP Data Routing

Data loading is two loads per line, maximum. Routing should be performed using a T–topology, as shown in Ref Drwg below:

Reference Drawing



Byte–ordering (along with the respective Data Mask, DQM) within the SDRAM/SGRAM should be swapped to optimize routing.

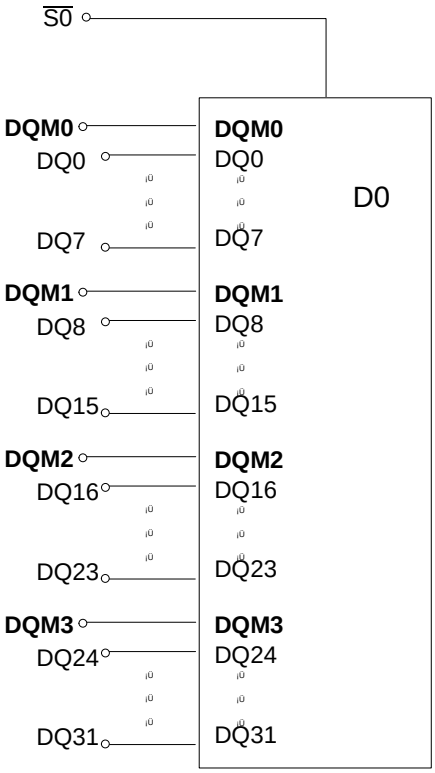
Module Byte	Front–Side Memory Byte	Back–Side Memory Byte	n value
BYTE 0	Memory B; BYTE 0	Memory D; BYTE 3	n = 115 pS
BYTE 1	Memory B; BYTE 3	Memory D; BYTE 0	n = 35 pS
BYTE 2	Memory B; BYTE 1	Memory D; BYTE 2	n = 35 pS
BYTE 3	Memory B; BYTE 2	Memory D; BYTE 1	n = 115 pS
BYTE 4	Memory A; BYTE 1	Memory C; BYTE 2	n = 115 pS
BYTE 5	Memory A; BYTE 2	Memory C; BYTE 1	n = 35 pS
BYTE 6	Memory A; BYTE 0	Memory C; BYTE 3	n = 35 pS
BYTE 7	Memory A; BYTE 3	Memory C; BYTE 0	n = 115 pS

FIGURE 4.5.8–F
QFP DATA ROUTING

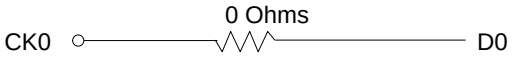
TSOP Layout Considerations

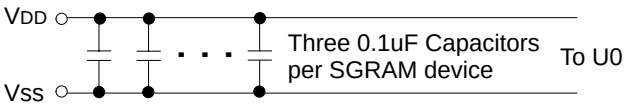
The assumed loading for this configuration is:

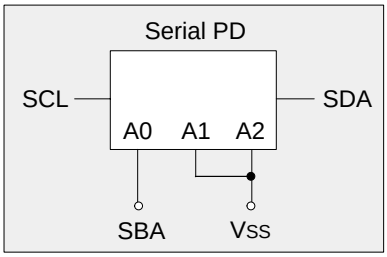
Signal	**32–bit**		**64–bit**	
	Single–sided	**Double–sided**	**Single–sided**	**Double–sided**
clocks	2 load	2 load	4 loads	4 loads
address/control	2 load	4 loads	4 loads	8 loads
data	1 load	2 loads	1 load	2 loads



This module configuration is approved using the following devices:
256K X 32 X 1 bank
256K X 32 X 2 banks
512K X 32 X 2 banks







* SPD is optional

FIGURE 4.5.8–G
256K, 512K, OR 1M X 32 SGRAM/SDRAM SO–DIMM BLOCK DIAGRAM

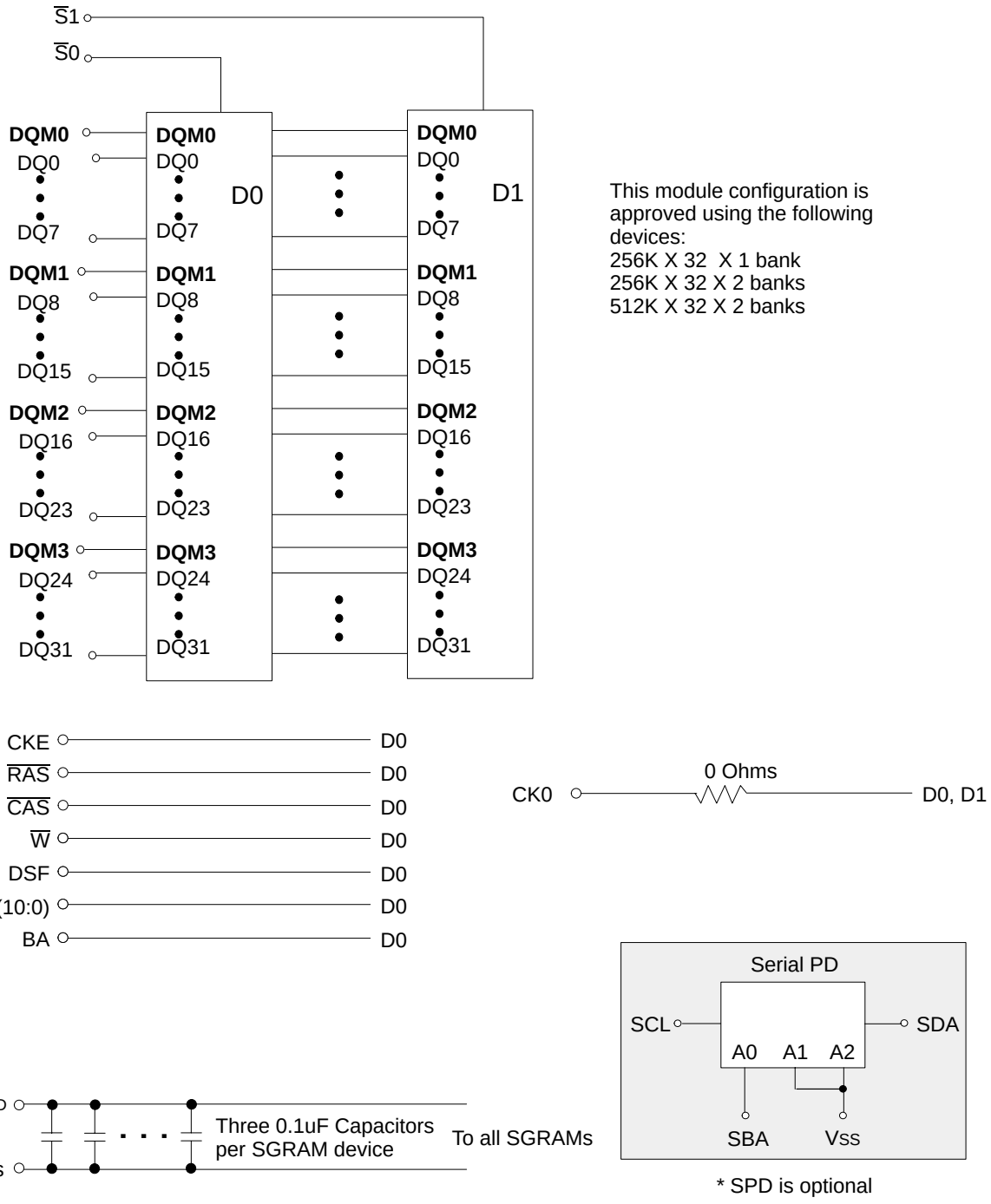


FIGURE 4.5.8–H
512K, 1M, OR 2M X 32 SGRAM/SDRAM SO–DIMM BLOCK DIAGRAM

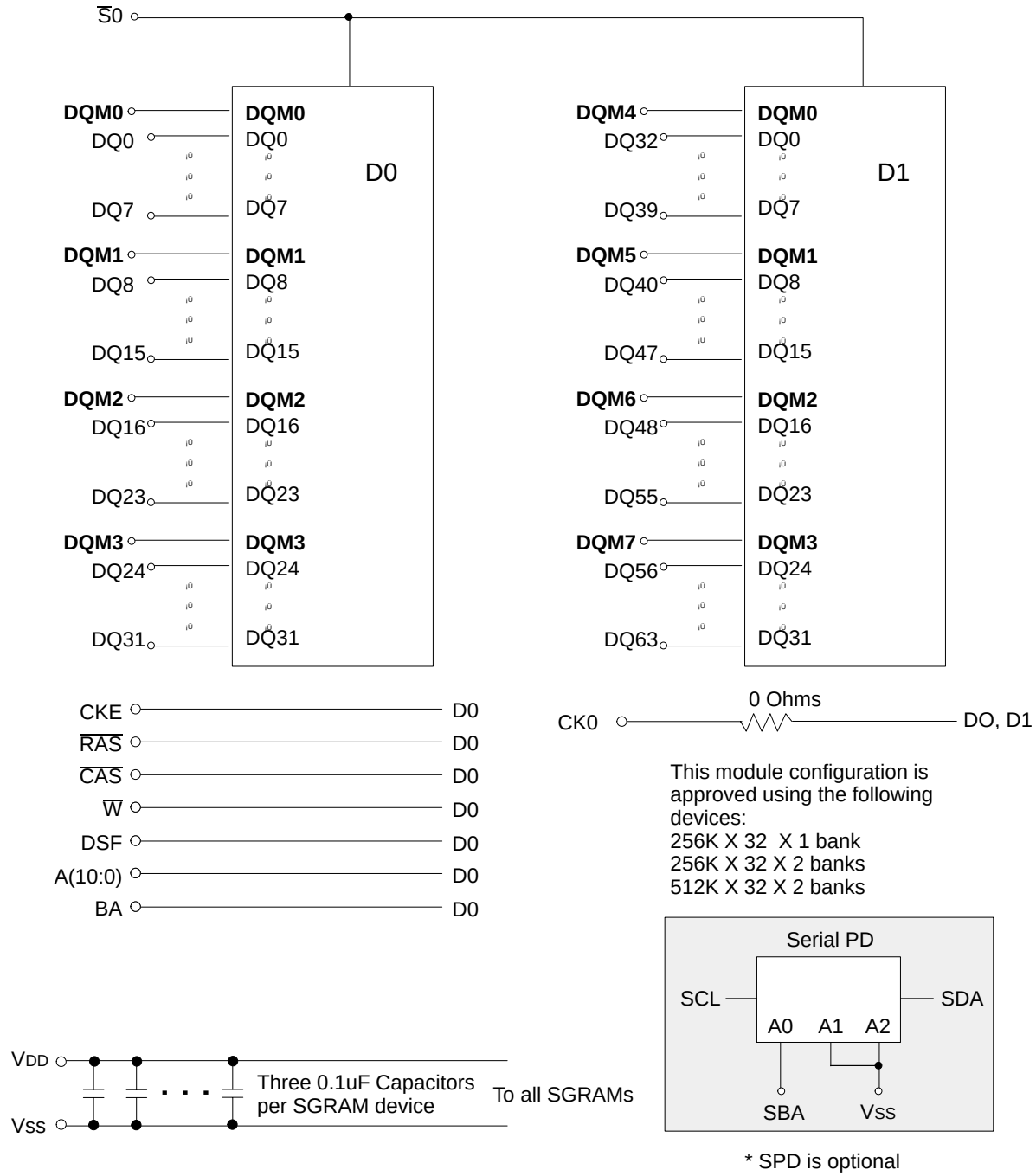


FIGURE 4.5.8–I
256K, 512K, OR 1M X 64 SGRAM/SDRAM SO–DIMM BLOCK DIAGRAM

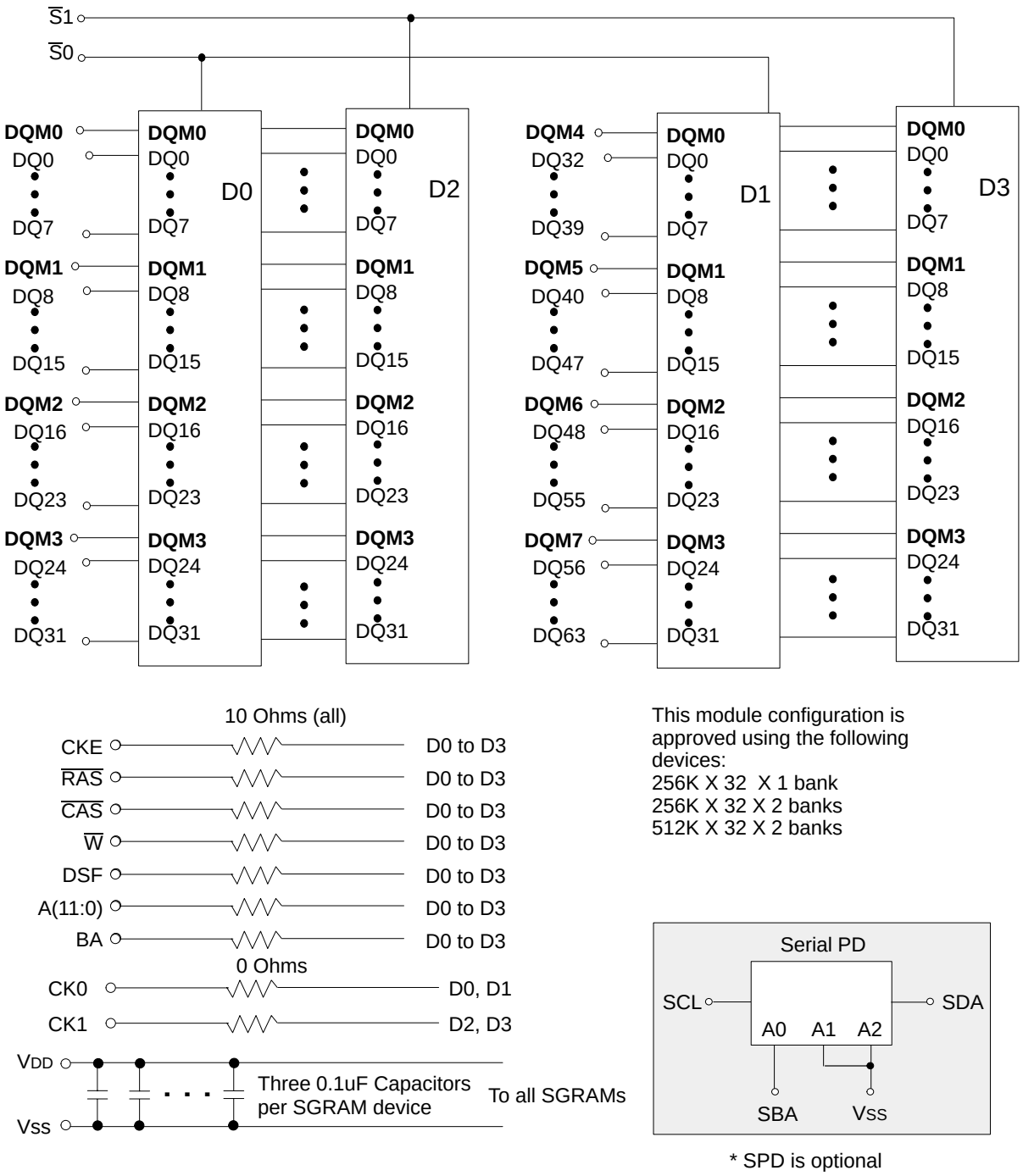


FIGURE 4.5.8–J
512K, 1M, OR 2M X 64 SGRAM/SDRAM SO–DIMM BLOCK DIAGRAM

Release 8r10